

Amendments to the Specification:

*AS
9/17/07*
Please replace paragraph [0019] beginning at page 10, line ~~8~~¹⁵ with the following amended paragraph:

--Thus, as shown in Fig. 3(d), even when a high-level clock signal is outputted from the oscillator 6 at intervals of a time period tb, the RS flip-flop 5 continues to output a low-level signal, as shown in Fig. 3(c), because a high-level signal is inputted from the comparator 4 to the reset terminal of the RS flip-flop 5, as shown in Fig. 3(e). Thus, the driver 1 keeps the MOS transistor Tr1 off and the MOS transistor Tr2 on.--

Please replace paragraph [0021] beginning at page 11, line ~~1~~⁵ with the following amended paragraph:

-- Thus, the driver 1 turns the MOS transistor Tr1 on and the MOS transistor Tr2 off, whereby a current begins to flow through the coil L, as shown in Fig. 3(a). As a result, the voltage VL inputted to the inverting input terminal of the comparator 4 is dropped by the current IL flowing through the coil L. As the current IL flowing through the coil L increases, as shown in Fig. 3(a), the voltage VL inputted to the inverting input terminal of the comparator 4 decreases, as shown in Fig. 3(b). When the voltage VL becomes lower than the voltage Vth from the level shifter 3, as shown in Fig. 3(b), the signal from the comparator 4 is switched to high level, as shown in Fig. 3(e). As a result, the signal from the RS flip-flop 5 turns to low level, as shown in Fig. 3(c).--

Please replace paragraph [0027] beginning at page 13, line ~~11~~⁸ with the following amended paragraph:

--Furthermore, as shown in Fig. 4, a resistance Ra is connected, at one end thereof, to the inverting input terminal of the comparator 4 and, at the other end thereof, to a node at which the source of the MOS transistor Tra and the drain of the MOS transistor Trb are connected together, and a constant-current power supply 11 that feeds a constant current is connected to the inverting

input terminal of the comparator 4. The other end of the constant-current power supply 11 is grounded. In this way, by connecting the resistance Ra and the constant-current power supply 11 together, a voltage drop $R_a \times I_{off}$ across the resistance Ra caused by the passage of a constant current I_{off} fed from the constant-current power supply 11 through the resistance Ra is added as an offset voltage V_{off} . That is, the resistance Ra and the constant-current power supply ~~10~~ 11 function as a voltage source 20.--

16
Please replace paragraph [0035] beginning at page 16, line ~~4~~ with the following amended paragraph:

--As is the case of the first embodiment, also in this embodiment, when a heavy load is connected as described above, the voltage obtained by detecting the current I_L flowing through the coil L is sufficiently higher than the offset voltage V_{xoff} from the voltage source 20a. That is, the voltage values V_{hoff} and V_{loff} added as an offset voltage V_{xoff} each fall within the voltage range in which the influence thereof on the voltage V_L inputted to the inverting input terminal of the comparator 4 is so small that it can be ignored.--

9/17/07

1
Please replace paragraph [0042] beginning at page 19, line ~~8~~ with the following amended paragraph:

--When a current detection circuit 10 having the same configuration as that shown in Fig. 4 of the first embodiment is incorporated in the switching power supply apparatus described above, the relation of connection between the current detection circuit 10 and the comparator 4 is shown in Fig. 8. In this case, as shown in Fig. 8, a resistance Ra used for adding an offset voltage V_{off} is replaced with a variable resistance Rb that can switch a resistance value depending on the output of the comparator 4. That is, the variable resistance Rb and the constant-current power supply 11 constitute a voltage source ~~21a~~ 20a. Other circuit blocks are the same as those in Fig. 4.--

**Please replace paragraph [0053] beginning at page 23, line 3 with the following
amended paragraph:**

--When the slope compensation voltage V_{slope} from the voltage source 21 decreases from a maximum value V_{Smax} to a minimum value of zero, as shown in Fig. 11(f), immediately before a clock is outputted from the oscillator 5 6, as shown in Fig. 11(c), the voltage V_{th} outputted from the level shifter 3 becomes lower than the voltage V_L , as shown in Fig. 11(b). That is, when the value of the voltage V_L fed to the inverting input terminal of the comparator 4 increases by changing from $V_{cc} - V_{off} - V_{Smax}$ to $V_{cc} - V_{off}$, as shown in Fig. 11(b), the voltage V_{th} becomes lower than the voltage value given by $V_{cc} - V_{off}$ --

15
9/17/07

**Please replace paragraph [0054] beginning at page 23, line 4 with the following
amended paragraph:**

--At this time, as shown in Fig. 11(e), a low-level signal is outputted from the comparator 4, and, immediately after the slope compensation voltage V_{slope} decreases from a maximum value V_{Smax} to a minimum value of zero, a high-level clock signal is outputted from the oscillator 6, as shown in Fig. 7(d) 11(d). Thus, a high-level signal is inputted to the set terminal of the RS flip-flop 5 after a low-level signal is inputted to the reset terminal thereof, whereby the signal from the RS flip-flop 5 is switched to high level, as shown in Fig. 11(c). On the other hand, after the slope compensation voltage V_{slope} reaches to a minimum value of zero, it gradually increases again, as shown in Fig. 11(f). Thus, as shown in Fig. 11(b), as the slope compensation voltage V_{slope} increases, the voltage V_L fed to the inverting input terminal of the comparator 4 decreases.--

**Please replace paragraph [0057] beginning at page 25, line 12 with the following
amended paragraph:**

--When a current detection circuit 10 having the same configuration as that shown in Fig. 4 of the first embodiment is incorporated in the switching power supply apparatus described above, the relation of connection between the current detection circuit 10 and the comparator 4 is